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FIGURE 1 -- PROGRAMMABLE PULSE SEQUENCER

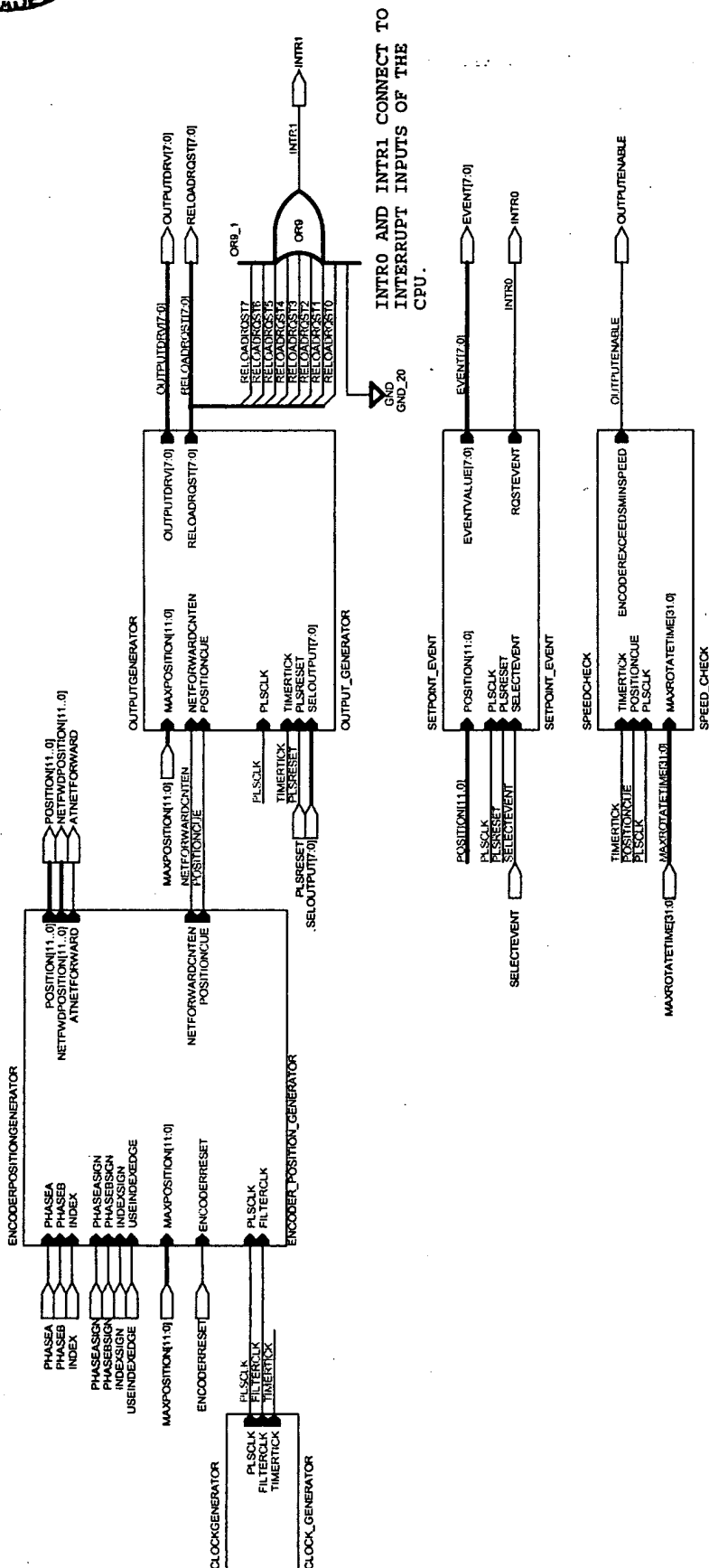


FIGURE 2 -- CLOCK GENERATOR

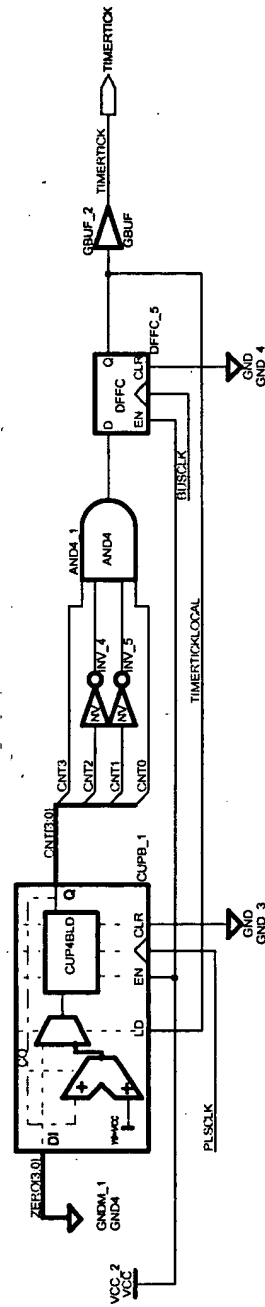
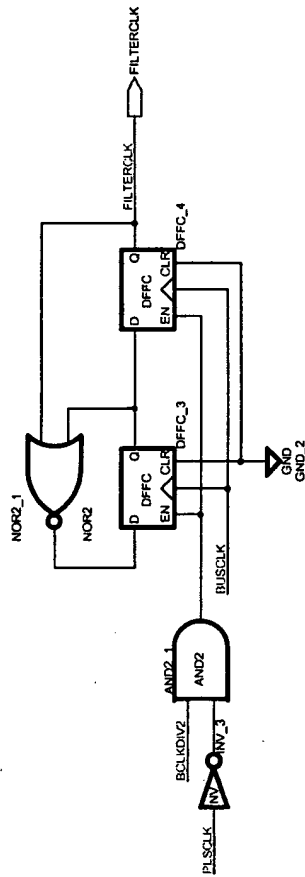




FIGURE 4 -- FAST SIGNAL DEBOUCE

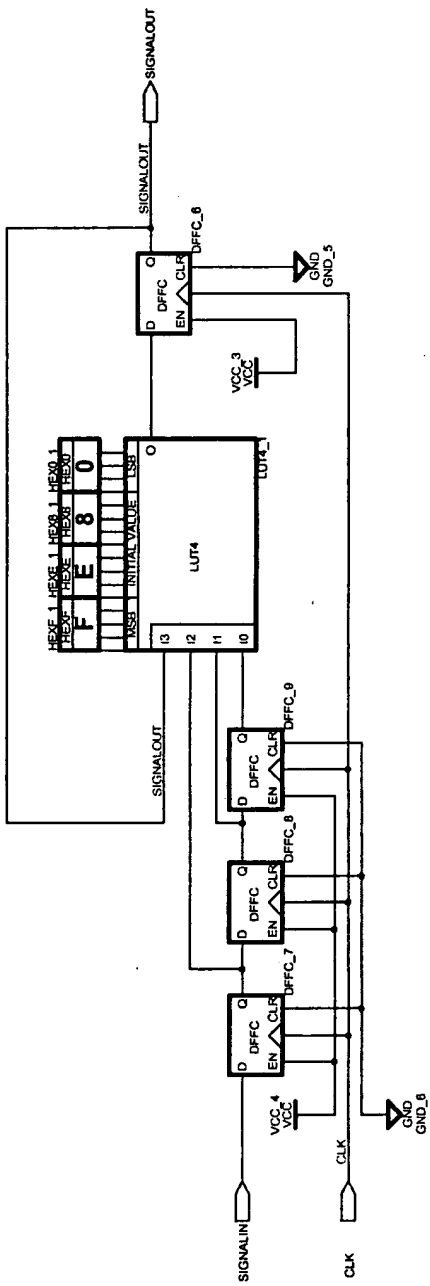


FIGURE 5 -- QUADRATURE CONVERTER

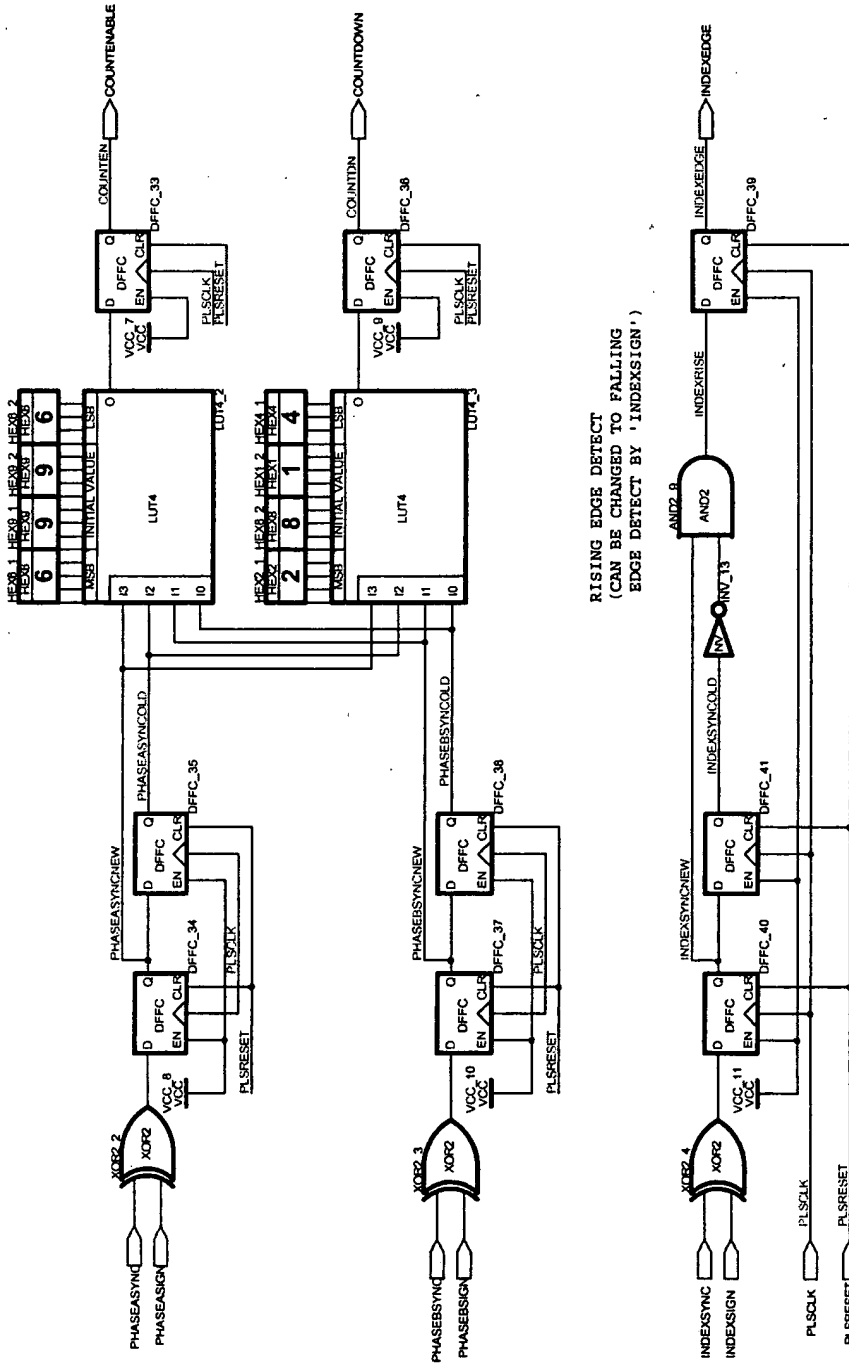


FIGURE 6 -- ENCODER POSITION COUNTER WITH NET FORWARD POSITION REGISTER

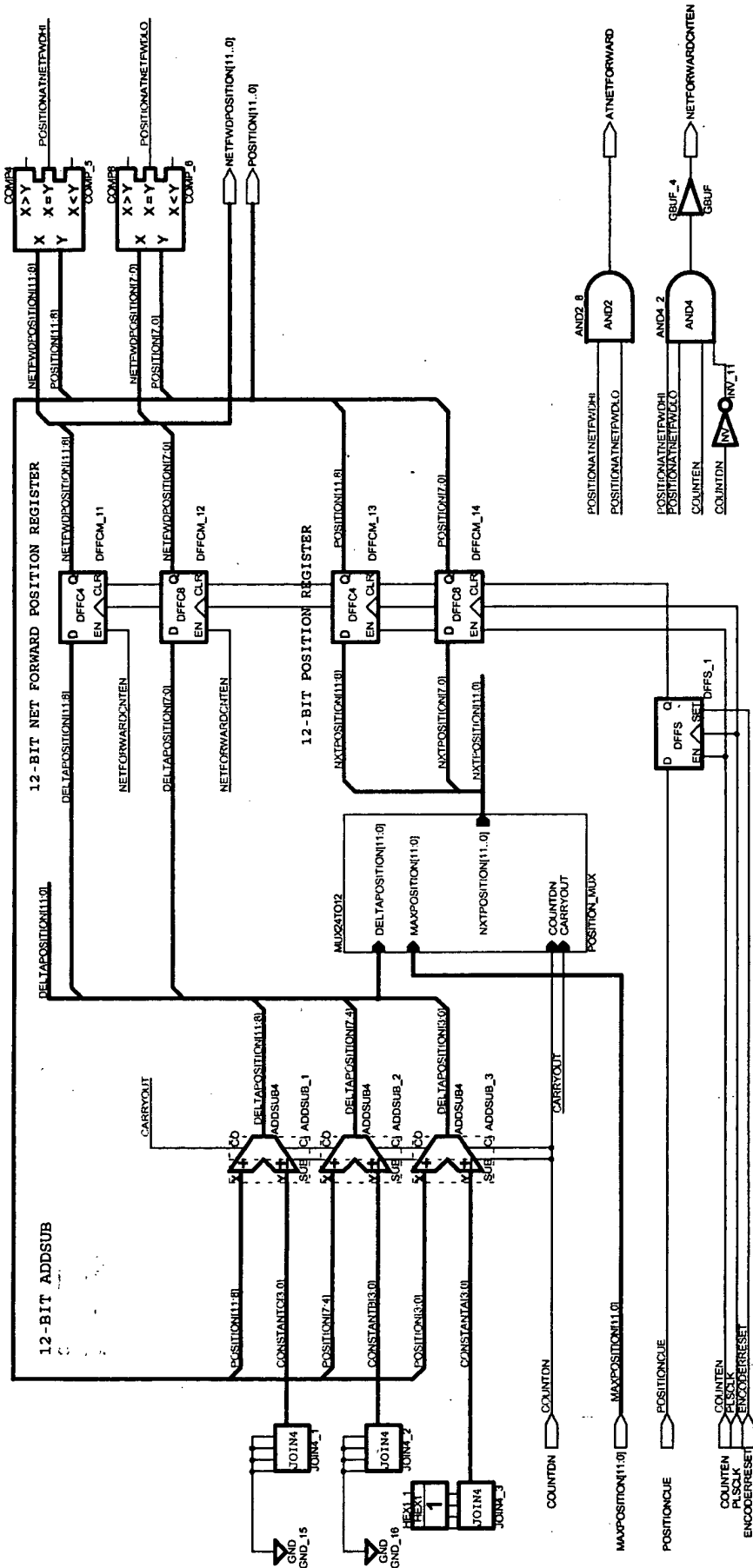


FIGURE 7 -- POSITION MULTIPLEXOR

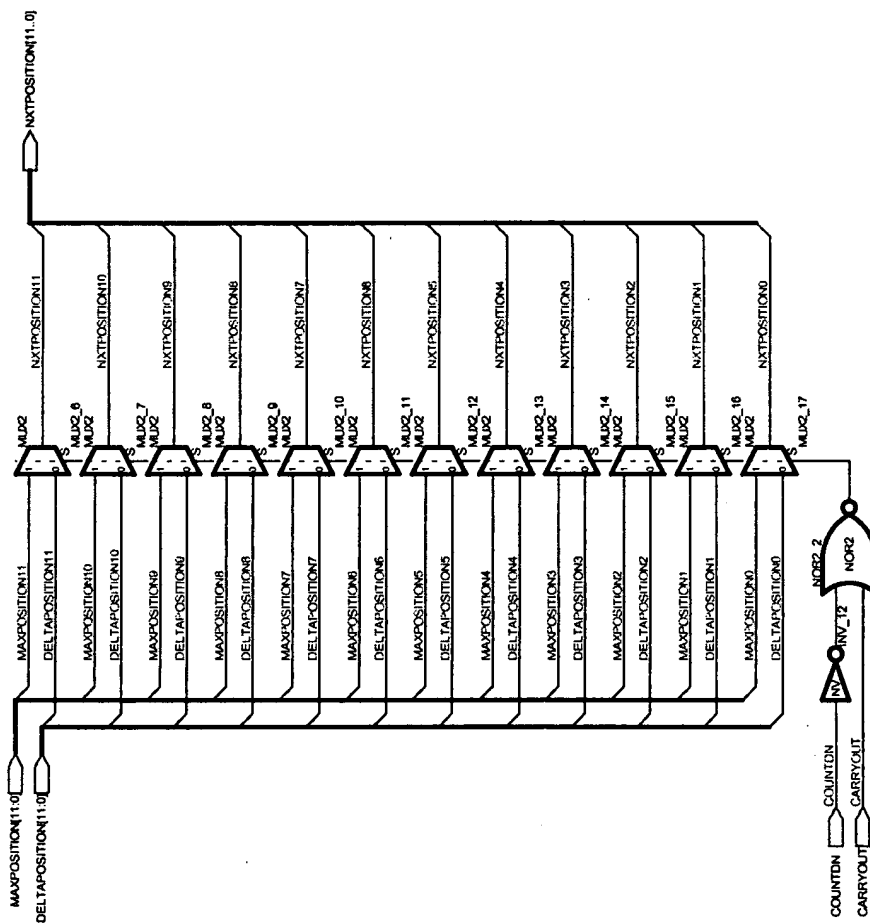




FIGURE 8 -- OUTPUT GENERATOR

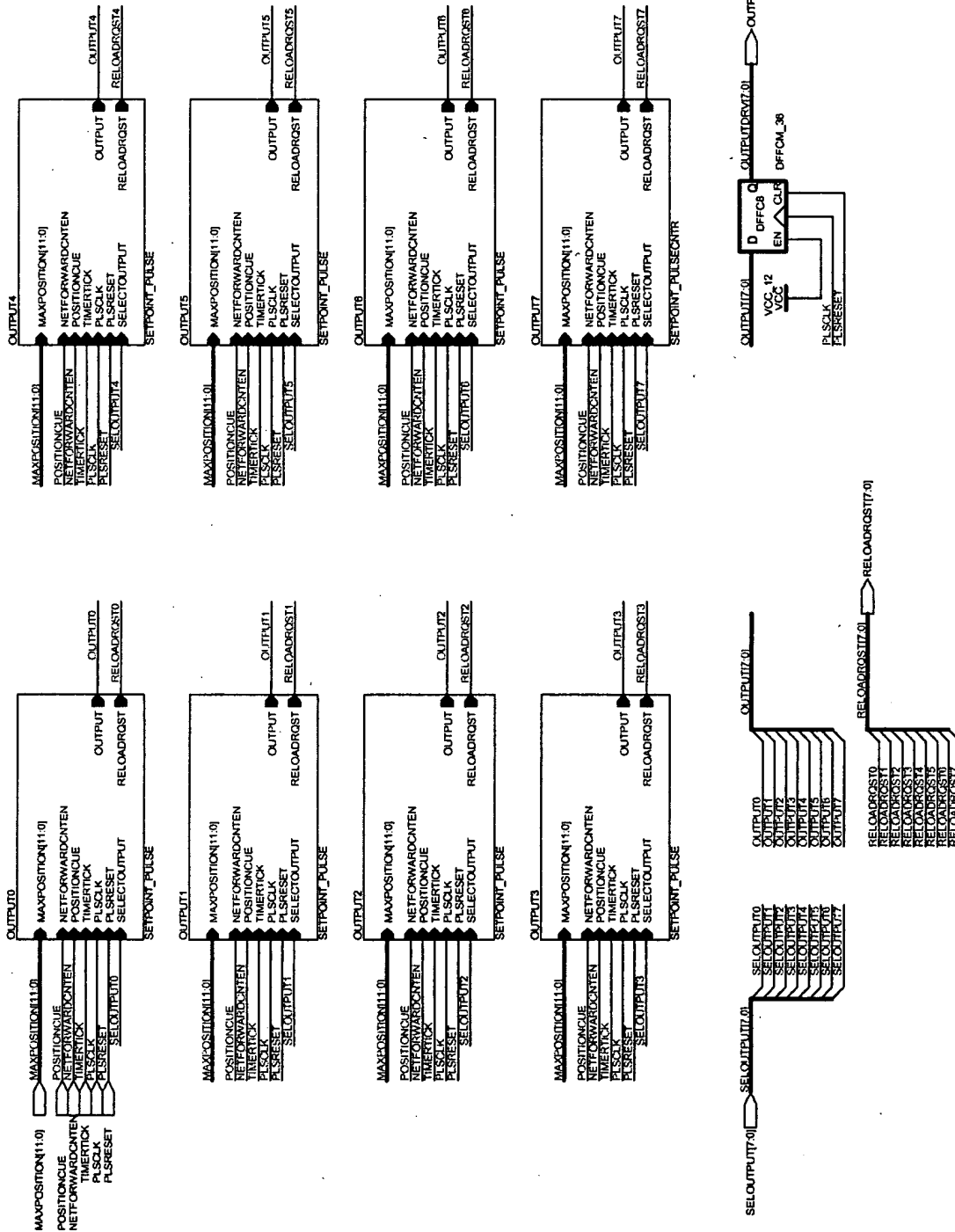


FIGURE 9 -- SETPOINT PULSE MODULE

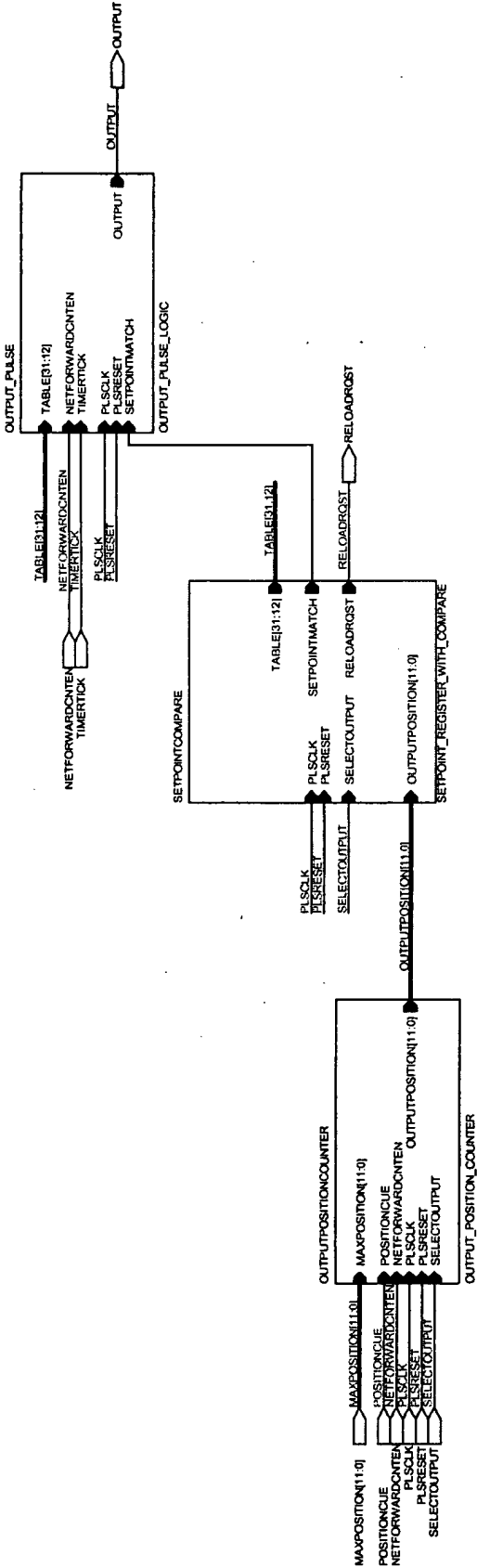
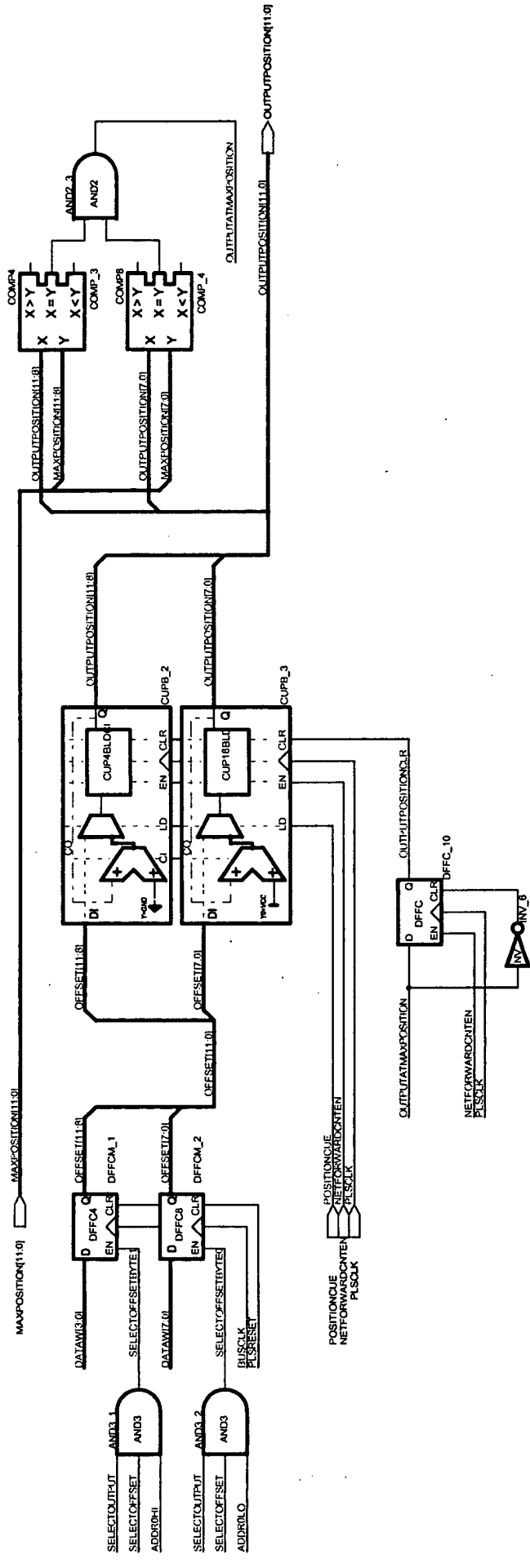
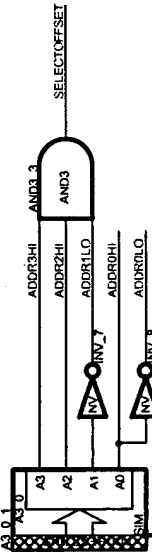


FIGURE 10 -- OUTPUT POSITION COUNTER



PROCESSOR ADDRESS BUS

OFFSET REGISTERS --  
ADDRESSES 12 TO 13



PROCESSOR DATA BUS

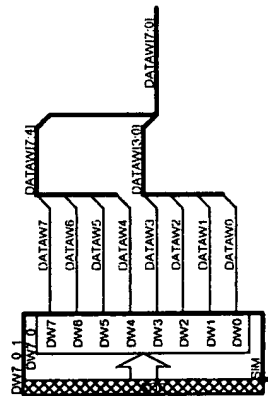
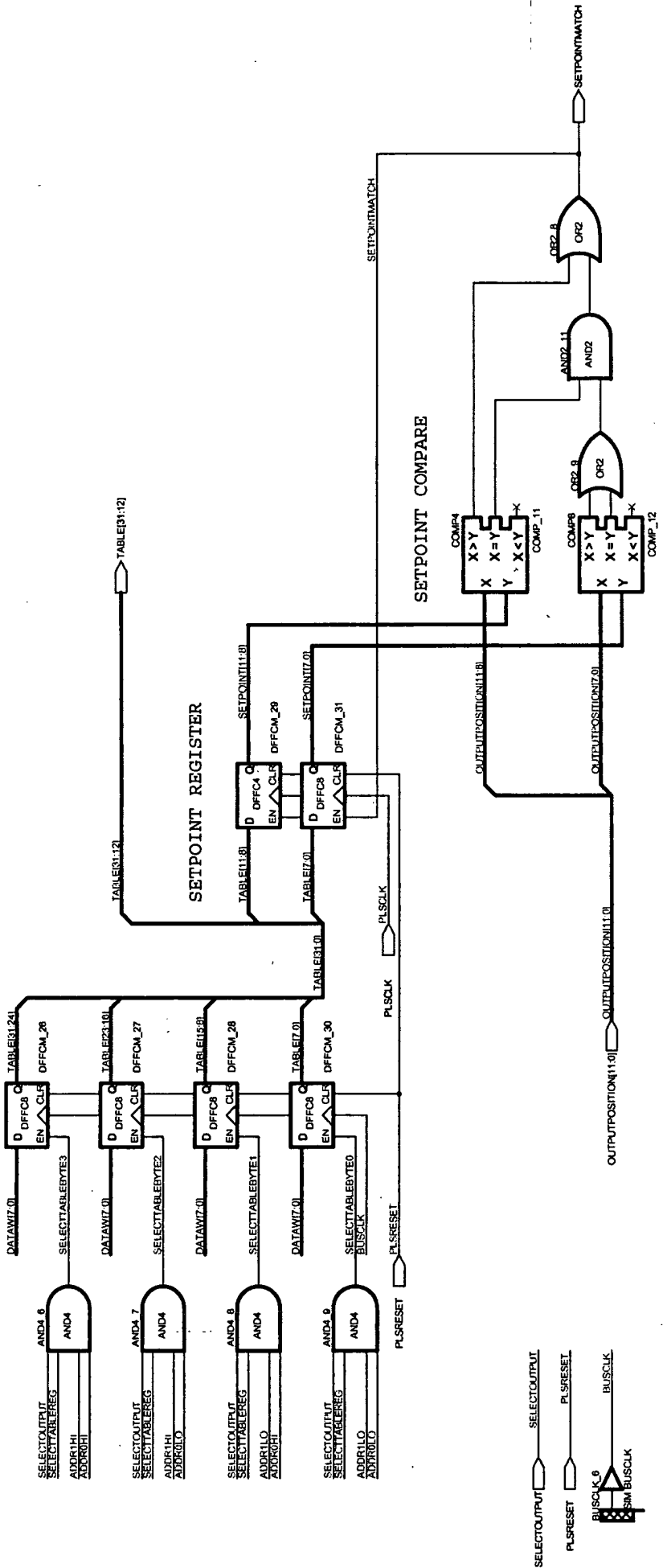
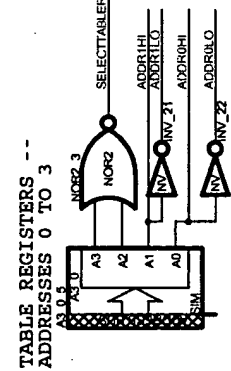


FIGURE 11 -- SETPOINT REGISTER WITH COMPARE

TABLE REGISTERS



PROCESSOR ADDRESS BUS



PROCESSOR DATA BUS

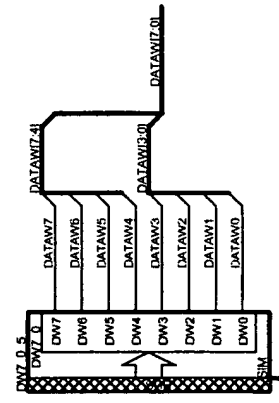
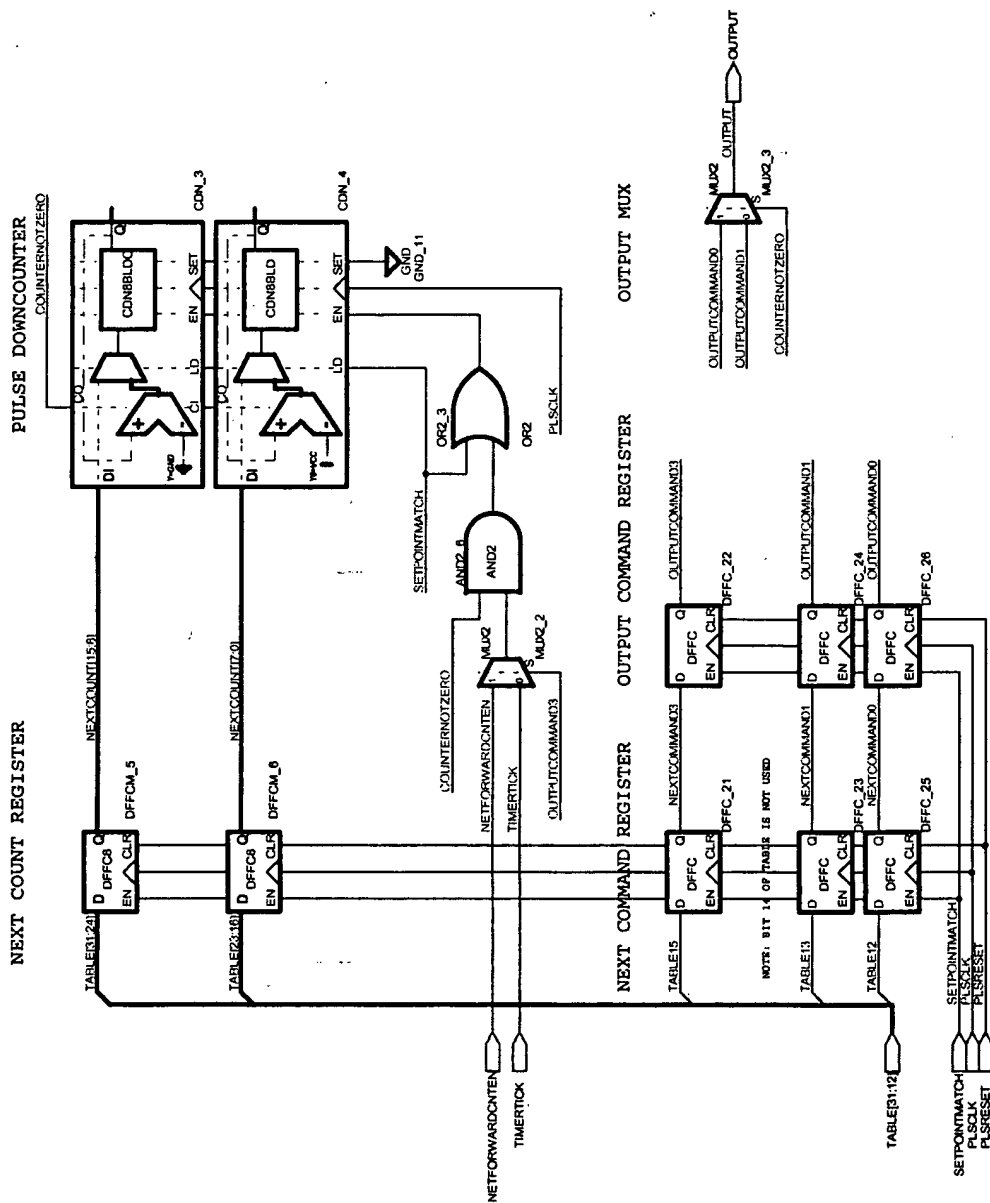


FIGURE 12 -- OUTPUT PULSE LOGIC



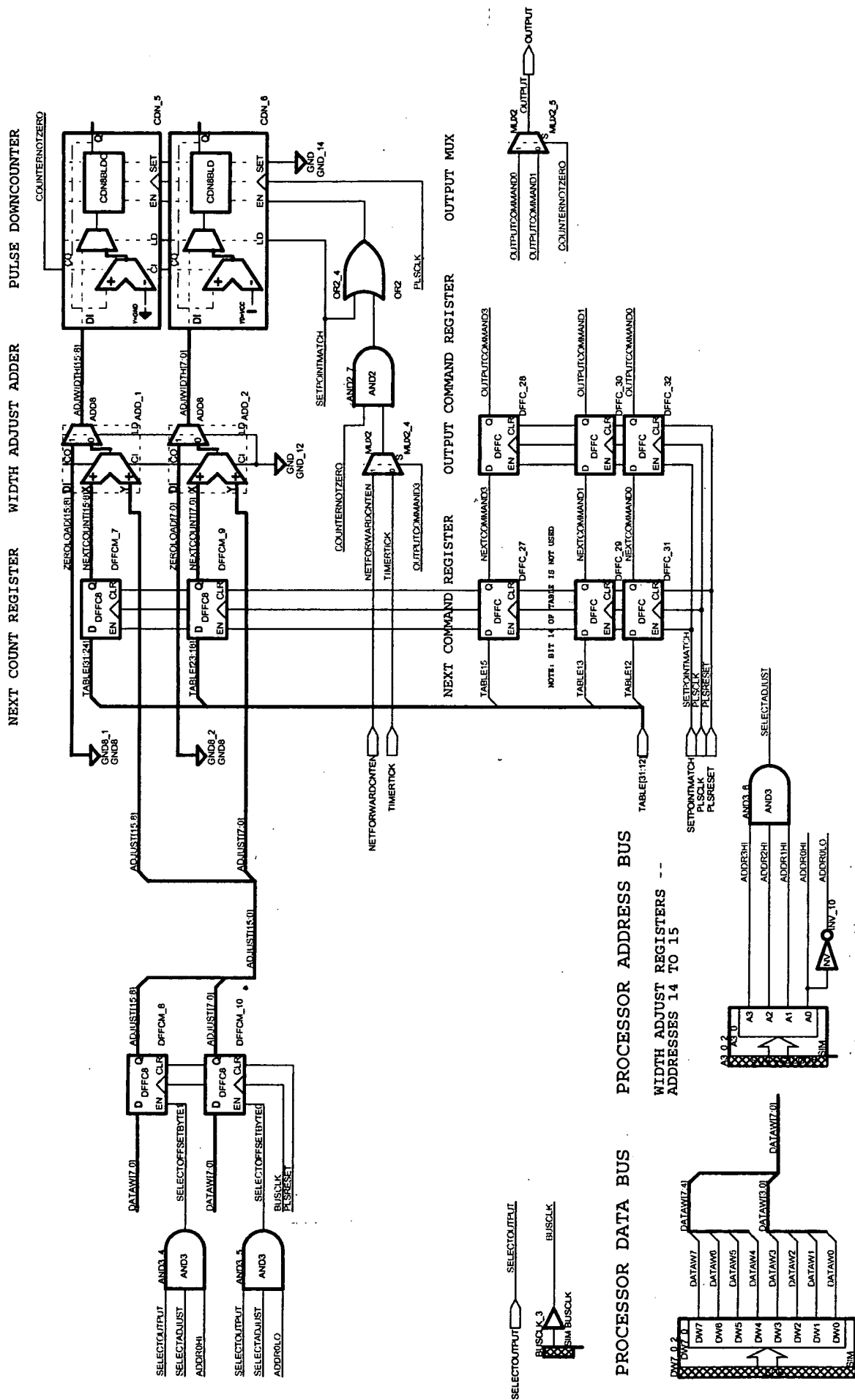


FIGURE 14 -- SETPOINT PULSE MODULE WITH OUTPUT PULSE COUNTER

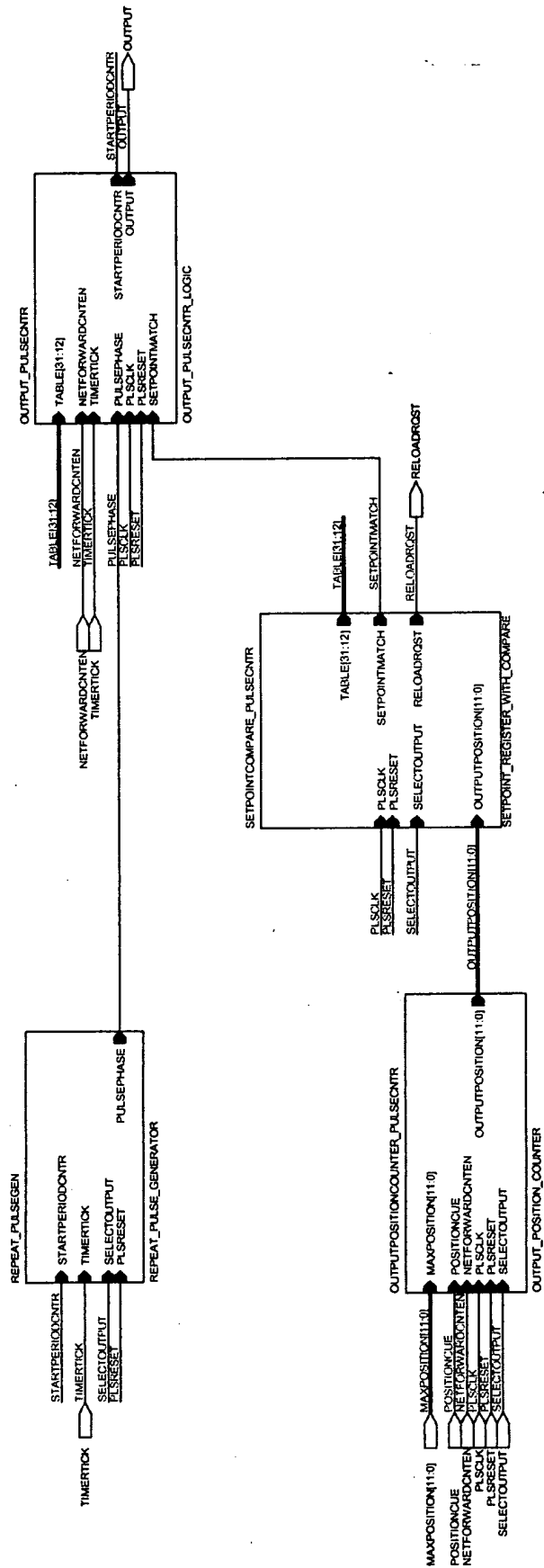


FIGURE 15 -- REPEAT PULSE GENERATOR

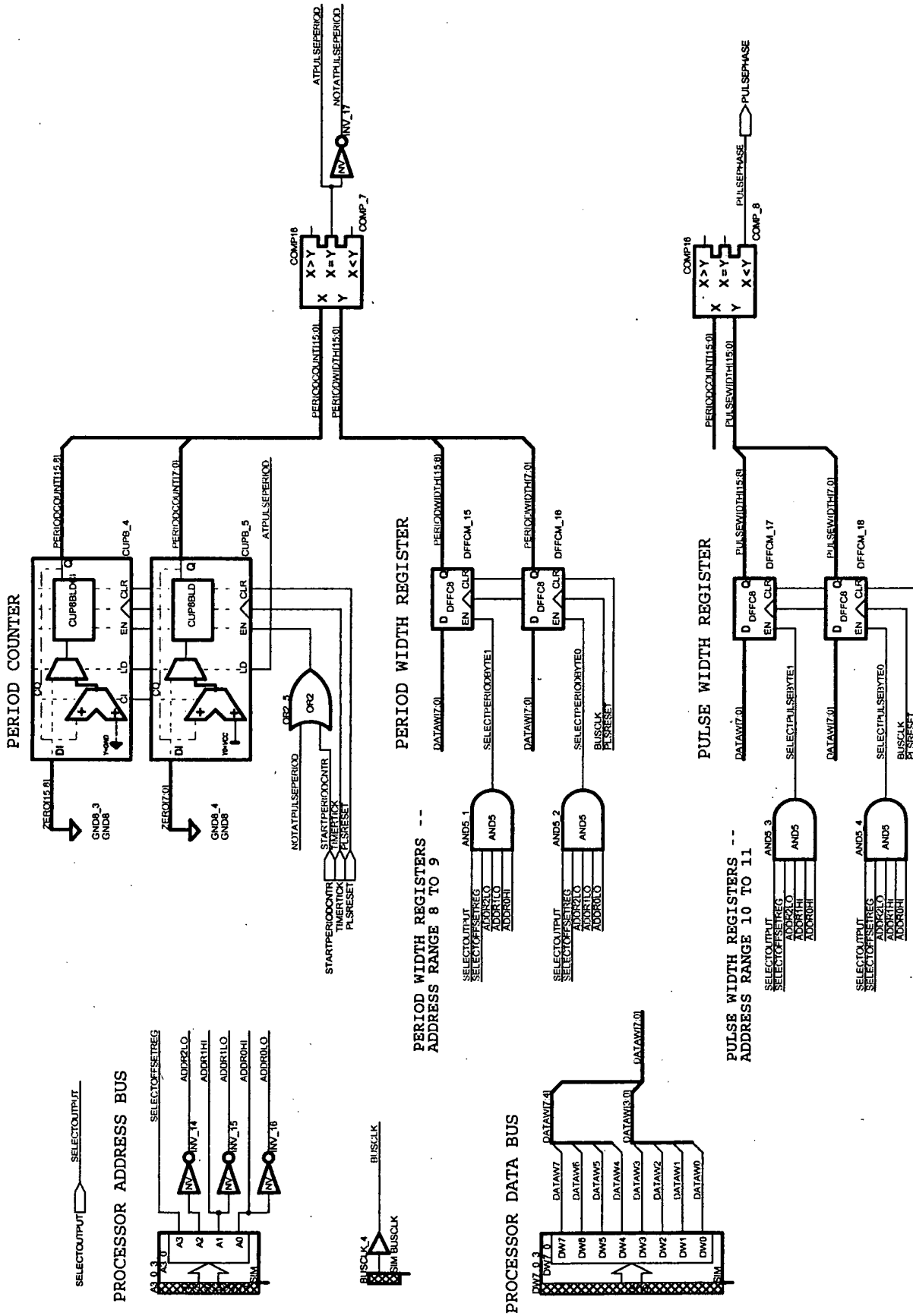




FIGURE 16 -- OUTPUT PULSE CNTR LOGIC

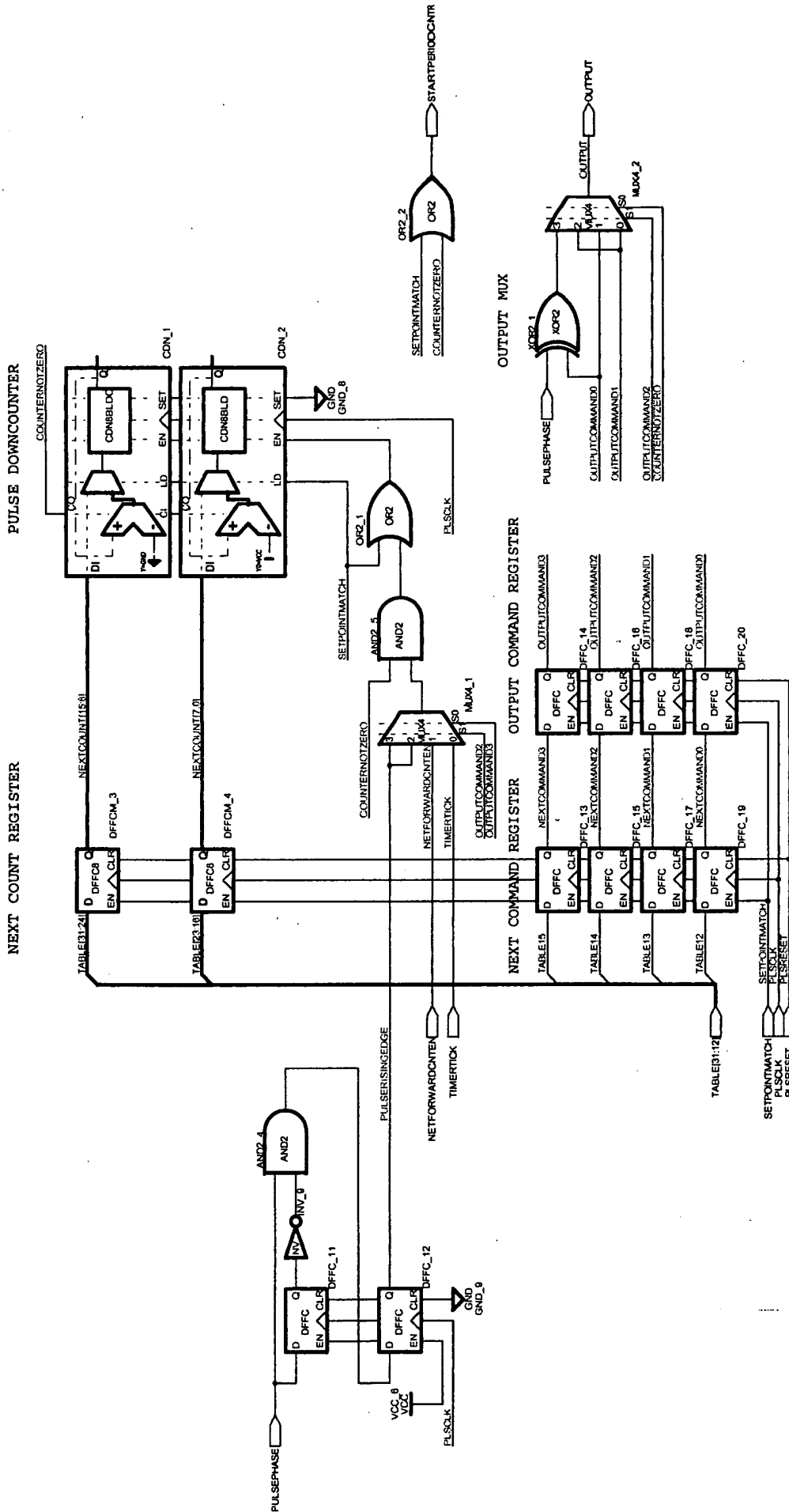


FIGURE 17 -- SET POINT EVENT

